

IN THE CLAIMS

Please cancel claims 1-17 without prejudice and add the following new claims:

1 18. (new) An arbiter for a system having a plurality of bus masters each
2 having real-time requirements for mastership of a bus, said arbiter comprising means
3 for allocating bus mastership to a given bus master as a percentage of the total bus
4 time.

1 19. (new) The arbiter according to claim 18 further comprising means for
2 allocating priority levels for bus mastership when said given bus master does not
3 request bus mastership during its allocated bus mastership.

1 20. (new) A system comprising:
2 a bus;
3 a plurality of bus masters each having real-time requirements for mastership
4 of the bus; and
5 an arbiter including means for allocating bus mastership to a given bus master
6 as a percentage of the total bus time.

1 21. (new) The system according to claim 20, said arbiter further including
2 means for allocating priority levels for bus mastership when said given bus master
3 does not request bus mastership during its allocated bus mastership.

1 22. (new) A QMS system supporting a plurality of queue users using a
2 bus, each queue user being a bus master having real-time requirements for
3 mastership of the bus, said QMS system comprising:
4 an arbiter including means for allocating mastership of the bus to a given bus
5 master, said mastership allocated as a percentage of the total bus time.

1 23. (new) The QMS system according to claim 22, said arbiter further
2 including means for allocating priority levels for bus mastership when said given bus
3 master does not request bus mastership during its allocated bus mastership.

1 24. (new) The QMS system according to claim 23, further comprising a
2 queue portal for each of the queue users, a respective queue user interface being
3 positioned between each queue user and its corresponding queue portal.

1 25. (new) The QMS system according to claim 24, said QMS further
2 comprising a memory for storing data as said data passes through said QMS;
3 wherein one of the queue users is a processor.

1 26. (new) The QMS system according to claim 25, said arbiter further
2 including a state machine for allocating to each bus master its percentage of the total
3 bus time.

1 27. (new) The QMS system according to claim 26, wherein said state
2 machine determines an active queue portal arbitration by cycling through a
3 predetermined number of states, in a fixed order or every clock cycle, each of said
4 states being associated with a respective queue portal.

1 28. (new) The QMS system according to claim 27, wherein said
2 percentage of total bus time allocated to a given queue user is determined by a total
3 number of states associated with a given queue portal corresponding to said given
4 queue user.

1 29. (new) The QMS system according to claim 28, wherein, when a given
2 state is active and the given queue user corresponding to said given queue portal
3 associated with said given state does not request bus mastership, then said means
4 for allocating priority levels for bus mastership is activated.

1 30. (new) The QMS system according to claim 29, wherein said arbiter
2 allocates the highest priority level to bus accesses by a non-interruptible memory
3 sequence triggered by the processor.

1 31. (new) The QMS system according to claim 30, wherein said arbiter
2 allocates a second highest priority level to bus accesses by the processor.

1 32. (new) The QMS system according to claim 32, wherein said arbiter
2 allocates a third highest priority level to bus accesses by said QMS.

3 33. (new) The QMS system according to claim 23, said arbiter further
4 including a state machine for allocating to each bus master its percentage of the total
5 bus time.

1 34. (new) The QMS system according to claim 33, wherein said state
2 machine determines an active queue portal arbitration by cycling through a
3 predetermined number of states, in a fixed order or every clock cycle, each of said
4 states being associated with a respective queue user.

1 35. (new) The QMS system according to claim 34, wherein said
2 percentage of total bus time allocated to a given queue user is determined by a total
3 number of states associated with the given queue user.

1 36. (new) The QMS system according to claim 35, wherein, when a given
2 state is active and the given queue user associated with said given state does not
3 request bus mastership, then said means for allocating priority levels for bus
4 mastership is activated.

1 37. (new) A QMS system supporting a plurality of queue users using a
2 bus, each queue user being a bus master having requirements for mastership of the
3 bus, said QMS system comprising:

4 a plurality of queue portals, each queue user being associated with a
5 corresponding queue portal; and

6 an arbiter including:

7 means for allocating bus mastership to a given queue user as a
8 percentage of total bus time, said means for allocating bus mastership having
9 a state machine,

10 wherein said state machine cycles through a predetermined number of
11 states, each of said states being associated with a corresponding queue
12 portal and thus also being associated with a corresponding queue user

13 associated with said corresponding queue portal, and further
14 wherein, when a given state is active, the corresponding queue user
15 associated with said corresponding queue portal associated with said given
16 state is allocated bus mastership, and still further
17 wherein said percentage of total bus time allocated to said given queue
18 user is determined by the total number of states associated therewith as
19 compared to the total number of states; and
20 means for allocating priority levels for bus mastership which is
21 activated when the queue user associated with a specific state does not
22 request bus mastership when said specific state is active.

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1 38. (new) A Bluetooth baseband peripheral comprising:
2 a QMS system according to one of claims 22-37;
3 a re-usable microprocessor block;
4 link control hardware for communication with Bluetooth devices via a radio IC
5 and a QMS system; and
6 an interface block between the bus and said re-usable microprocessor block,
7 the queue users comprising:
8 a communication control block;
9 a host queue user;
10 a voice encoder/decoder; and
11 a processor forming part of said re-usable microprocessor block,
12 wherein each of said queue users is connected to the bus via its queue
13 user interface and a respective bus master and bus tri-state driver.

1 39. (new) A Bluetooth baseband peripheral comprising:
2 a QMS system according to one of claims 22, 23, 28, 29, 32, 35, 36, and 37;
3 a re-usable microprocessor block;
4 link control hardware for communication with Bluetooth devices via a radio IC
5 and a QMS system; and
6 an interface block between the bus and said re-usable microprocessor block.

1 40. (new) The Bluetooth baseband peripheral according to claim 39, wherein
2 the queue users is one or more of a communication control block, a host queue user,

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(new) The Bluetooth baseband peripheral according to claim 39, wherein the queue users is one or more of a communication control block, a host queue user, a voice encoder/decoder, and a processor forming part of said re-usable microprocessor block, and further

wherein each of said queue users is connected to the bus via its queue user interface and a respective bus master and bus tri-state driver.

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(new) A Bluetooth baseband peripheral comprising:
a QMS system according to one of claims 22, 23, 29, 36, and 37; and
link control hardware for communication with Bluetooth devices via a radio IC
and a QMS system.

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